CLAIMS

1. A low-pass filter comprising:

first filtering means that accepts, as an input, an input signal to said low-pass filter and outputs a first voltage;

a circuit element included in said first filtering means for allowing a first current to flow in accordance with said first voltage;

current generating means for generating a second current at a given rate to said first current;

second filtering means that accepts, as an input, said second current and outputs a second voltage; and

adding means for adding said first voltage and said second voltage and outputting an output signal of said low-pass filter.

2. The low-pass filter of Claim 1,

wherein said given rate is a positive number smaller than 1.

3. The low-pass filter of Claim 1,

wherein said current generating means is a current mirror circuit that has, on an input side thereof, a first semiconductor element with first conductance, and on an output side thereof, a second semiconductor element with second conductance at said given rate to said first conductance, accepts, as an input, said first current and outputs said second current, and

said circuit element is said first semiconductor element.

4. The low-pass filter of Claim 3,

wherein said circuit element is a resistive element with a resistance value corresponding to said first conductance instead of said first semiconductor element, and

said current mirror circuit accepts, as the input, a third current corresponding to

said first current instead of said first current.

5. The low-pass filter of Claim 1,

wherein said circuit element is a first voltage-current converter with first conductance for converting said first voltage into said first current, and

said current generating means is a second voltage-current converter with second conductance at said given rate to said first conductance for converting said first voltage into said second current.

6. The low-pass filter of Claim 1,

wherein said adding means is an operational amplifier that has said second filtering means in a negative feedback portion thereof, accepts, as an input, said first voltage at a non-inverting input terminal thereof and outputs a third voltage as said output signal.

7. The low-pass filter of Claim 1,

wherein said adding means is an operational transconductance amplifier that accepts, as inputs, said first and second voltages and outputs a third current as said output signal.

8. The low-pass filter of Claim 3,

wherein said first semiconductor element is a first transistor that provides said first conductance in accordance with a supplied first bias current,

said second semiconductor element is a second transistor that provides said second conductance in accordance with a supplied second bias current, and

said first and second bias currents are changed in amplitudes thereof on the basis of a common bias control signal.

9. The low-pass filter of Claim 3,

wherein said current mirror circuit has, on an output side thereof, said second

through nth (wherein n is a natural number of 3 or more) semiconductor elements and includes switches for respectively switching outputs of currents flowing through said second through nth semiconductor elements, and

said switches allow one of or a sum of a plurality of the currents respectively flowing through said second through nth semiconductor elements to be output as said second current.

10. The low-pass filter of Claim 4,

wherein said first semiconductor element is a first transistor that provides said first conductance in accordance with a supplied first bias current,

said second semiconductor element is a second transistor that provides said second conductance in accordance with a supplied second bias current,

said first and second bias currents are changed in amplitudes thereof on the basis of a common bias control signal, and

said circuit element is, instead of said resistive element, a resistor ladder circuit that has a resistance value corresponding to said first conductance and is able to change said resistance value in accordance with change of said first conductance.

11. The low-pass filter of Claim 5,

wherein said first and second voltage-current converters respectively change said first and second conductance on the basis of a common bias control signal.

12. The low-pass filter of Claim 3,

wherein at least one of said first and second semiconductor elements is a transistor that provides at least one of said first and second conductance in accordance with a supplied bias current, and

said low-pass filter further comprises offset compensating means for adjusting said bias current on the basis of said output signal obtained with said first current cut off.

13. The low-pass filter of Claim 12,

wherein said offset compensating means includes voltage holding means for holding a voltage of said output signal obtained with said first current cut off, and adjusts said bias current on the basis of said voltage held by said voltage holding means.

14. The low-pass filter of Claim 12,

wherein said offset compensating means includes:

a comparator for comparing a voltage of said output signal obtained with said first current cut off with a reference voltage;

an updown counter for incrementing or decrementing a counter value thereof on the basis of an output of said comparator; and

a DA converter for converting said counter value into an analog value, and

said offset compensating means adjusts said bias current on the basis of an output of said DA converter.

15. The low-pass filter of Claim 3,

wherein said second semiconductor element is a transistor that provides said second conductance in accordance with a supplied bias current, and

said low-pass filter further comprises:

a replica circuit having an identical architecture to a portion including said second semiconductor element, said second filtering means and said adding means; and

offset compensating means for adjusting, on the basis of an output of said replica circuit, a bias current supplied to a transistor included in said replica circuit correspondingly to said second semiconductor element and said bias current supplied to said second semiconductor element.

16. The low-pass filter of Claim 15,

wherein said offset compensating means is an inverting amplifier with a given time constant.

17. The low-pass filter of Claim 3,

wherein said first semiconductor element is a first transistor that provides said first conductance in accordance with a supplied first bias current,

said second semiconductor element is a second transistor that provides said second conductance in accordance with a supplied second bias current, and

said low-pass filter further comprises bias adjusting means for adjusting said first and second bias currents in accordance with temperature change.

18. The low-pass filter of Claim 17,

wherein said bias adjusting means includes:

a third transistor corresponding to said first transistor; and

a fourth transistor corresponding to said second transistor, and

said bias adjusting means adjusts bias currents with a given current difference respectively supplied to said third and fourth transistors, in such a manner that a given voltage difference is caused between said third and fourth transistors, and adjusts said first and second bias current in accordance with the adjustment of said bias current.

19. The low-pass filter of Claim 17,

wherein said bias adjusting means is a temperature compensating circuit that changes said first and second bias currents in proportion to the temperature change.

20. The low-pass filter of Claim 1,

wherein said circuit element includes a first switched capacitor circuit and a second switched capacitor circuit having one end connected to one end of said first switched capacitor circuit and the other end connected to said second filtering means, and

allows said first current to flow when said first and second switched capacitor circuits are in a first connection state, and

said current generating means corresponds to said second switched capacitor circuit, has a capacitance value at said given rate to a sum of capacitance values of said first and second switched capacitor circuits, and generates said second current when said first and second switched capacitor circuits are in a second connection state.

21. The low-pass filter of Claim 20,

wherein said adding means includes a voltage follower circuit for accepting, as an input, said second voltage, and

said first filtering means outputs said first voltage on the basis of an output voltage of said voltage follower circuit.

22. The low-pass filter of Claim 20,

wherein at least one of said first and second switched capacitor circuits is connected to a third switched capacitor circuit in parallel, and

when one of said first or second switched capacitor circuit and said third switched capacitor circuit connected in parallel is electrically connected to a first terminal, the other is electrically connected to a second terminal.

23. A low-pass filter for accepting, as an input, a differential signal between first and second input signals and outputting a differential signal between first and second output signals, comprising:

a first low-pass filter unit for accepting said first input signal as an input and outputting said first output signal; and

a second low-pass filter unit for accepting said second input signal as an input and outputting said second output signal,

wherein at least one of said first and second low-pass filter units includes:

first filtering means that accepts, as an input, said first or second input signal and outputs a first voltage;

a circuit element included in said first filtering means for allowing a first current to flow in accordance with said first voltage;

current generating means for generating a second current at a given rate to said first current;

second filtering means that accepts, as an input, said second current and outputs a second voltage; and

adding means for adding said first voltage and said second voltage and outputting said first or second output signal.

24. The low-pass filter of Claim 23,

wherein said current generating means is a current mirror circuit that has, on an input side thereof, a first semiconductor element with first conductance, and on an output side thereof, a second semiconductor element with second conductance at said given rate to said first conductance, accepts said first current as an input and outputs said second current, and

said circuit element is said first semiconductor element.

25. The low-pass filter of Claim 23,

wherein said circuit element is a first voltage-current converter with first conductance for converting said first voltage into said first current, and

said current generating means is a second voltage-current converter with second conductance at said given rate to said first conductance for converting said first voltage into said second current.

26. A feedback system for feeding back an output clock, generated on the basis of an input clock, to make said output clock attain a desired characteristic, comprising:

a charge pump circuit for generating a charge current on the basis of a phase difference between said input clock and a clock resulting from the feedback;

a loop filter for accepting said charge current as an input; and

output clock generating means for generating said output clock on the basis of an output signal from said loop filter,

wherein said loop filter includes:

first filtering means for accepting said charge current as an input and outputting a first voltage;

a circuit element included in said first filtering means for allowing a first current to flow in accordance with said first voltage;

current generating means for generating a second current at a given rate to said first current;

second filtering means for accepting said second current as an input and outputting a second voltage; and

adding means for adding said first voltage and said second voltage and outputting said output signal.

27. The feedback system of Claim 26,

wherein said output clock generating means is a voltage controlled oscillator that oscillates said output clock and changes an oscillation frequency on the basis of said output signal from said loop filter.

28. The feedback system of Claim 26,

wherein said output clock generating means is a voltage controlled delay circuit that changes a delay of said output clock from said input clock on the basis of said input clock and said output signal from said loop filter.

29. The feedback system of Claim 26, further comprising:

a stationary phase error canceling circuit including a charge pump circuit for generating a third current on the basis of a phase difference between said input clock and said clock resulting from the feedback, charge storing means for accepting said third current, and a voltage controlled current source for generating a fourth current in accordance with a voltage generated in said charge storing means,

wherein said current generating means is a current mirror circuit that has, on an input side thereof, a first field effect transistor for providing first conductance in accordance with a supplied first bias current, and on an output side thereof, a second field effect transistor for providing second conductance at said given rate to said first conductance, accepts said first current on the input side thereof and said fourth current on one of the input and output sides thereof, and outputs said second current, and

said circuit element is said first field effect transistor.

30. The feedback system of Claim 26,

wherein said circuit element is capable of changing conductance thereof, and

said feedback system further comprises bias controlling means for changing said conductance of said circuit element and said charge current in accordance with a common bias control signal.

31. The feedback system of Claim 30,

wherein said current generating means is a current mirror circuit that has, on an input side thereof, a first field effect transistor for providing first conductance in accordance with a supplied first bias current, and on an output side thereof, a second field effect transistor for providing second conductance at said given rate to said first conductance in accordance with a supplied second bias current, accepts said first current as an input and outputs said second current,

said circuit element is said first field effect transistor, and

said bias controlling means changes said first and second bias currents and said charge current in accordance with said bias control signal.

32. The feedback system of Claim 30,

wherein said circuit element is a first voltage-current converter with first conductance for converting said first voltage into said first current,

said current generating means is a second voltage-current converter with second conductance at said given rate to said first conductance for converting said first voltage into said second current,

said first and second conductance of said first and second voltage-current converters are changeable, and

said bias controlling means changes said first and second conductance and said charge current in accordance with said bias control signal.

33. The feedback system of Claim 30,

wherein said bias control signal is generated on the basis of said output signal from said loop filter.

34. The feedback system of Claim 30,

wherein said adding means is an operational amplifier, and

said bias controlling means changes a band characteristic of said operational amplifier in accordance with said bias control signal.

35. The feedback system of Claim 33, further comprising:

startup means for switching said output signal from said loop filter between a first state where said output signal is set to an output from said adding means and a second state where said output signal is set to a given voltage,

wherein said startup means sets said second state at the startup of said feedback system.

36. The feedback system of Claim 35,

wherein said adding means is an operational amplifier that has said second filtering means in a negative feedback portion thereof, accepts, as an input, said first voltage at a non-inverting input terminal thereof and outputs a third voltage as said output signal,

said startup means has a switch for switching a connecting state of input terminals of said operational amplifier between short-circuit and disconnection, and

said switch disconnects said input terminals in said first state and short-circuits said input terminals in said second state.

37. The feedback system of Claim 35,

wherein said startup means has a switch for switching a power source for said given voltage between an internal power source and an external power source.

38. A feedback system for feeding back an output clock, generated on the basis of an input clock, to make said output clock attain a desired characteristic, comprising:

a charge pump circuit for generating first and second charge currents on the basis of a phase difference between said input clock and a clock resulting from the feedback;

a loop filter for accepting, as an input, a differential signal between said first and second charge currents and outputting first and second output signals; and

output clock generating means for accepting, as an input, a differential signal between said first and second output signals and generating said output clock,

wherein said loop filter includes:

a first low-pass filter for accepting, as an input, said first charge current and outputting said first output signal; and

a second low-pass filter for accepting said second charge current as an input and outputting said second output signal,

at least one of said first and second low-pass filters includes:

first filtering means for accepting, as an input, at least one of said first and second charge currents and outputting a first voltage;

a circuit element included in said first filtering means for allowing a first current to flow in accordance with said first voltage;

current generating means for generating a second current at a given rate to said first current;

second filtering means for accepting, as an input, said second current and outputting a second voltage; and

adding means for adding said first voltage and said second voltage and outputting at least one of said first and second output signals.

39. A semiconductor integrated circuit comprising the low-pass filter according to Claim 1.

40. A semiconductor integrated circuit comprising the feedback system according to Claim 26.

41. The semiconductor integrated circuit of Claim 40 used in an IC card.

42. The semiconductor integrated circuit of Claim 40,

wherein said semiconductor integrated circuit has a chip-on-chip structure, and

said feedback system is included in an upper portion of said chip-on-chip structure.

43. The semiconductor integrated circuit of Claim 40,

wherein said feedback system is provided on a pad region of said semiconductor integrated circuit.

44. The semiconductor integrated circuit of Claim 40,

wherein said semiconductor integrated circuit is a microprocessor.